AMENDMENTS TO THE CLAIMS

Claims 1-20 (Cancelled)

21. (New) A transmission gate, comprising:

a switch circuit including an input that is coupled to an input node, an output that is coupled to an output node, and a control input that is coupled to a control input node;

a boost circuit that is arranged to provide a boost voltage at a boost node responsive to a supply voltage;

a current source circuit that is coupled between the boost node and the control input node, wherein the current source circuit is arranged to provide a bias current during an on condition; and

a constant voltage difference circuit that is coupled to the control input node, wherein the constant voltage difference circuit is arranged to provide a control input voltage at the control input node such that a voltage difference between the control input voltage and an input voltage at the input node is substantially constant during the on condition.

22. (New) The transmission gate of Claim 21, wherein the constant voltage difference circuit is coupled between the input node and the control input node, and wherein the constant voltage difference circuit includes at least one of a diode and a transistor.

23. (New) The transmission gate of Claim 21, wherein the constant voltage difference circuit includes a plurality of transistors, and wherein the constant voltage difference circuit is arranged such that the substantially constant voltage difference is substantially equal to the sum of the gate-to-source voltages of each of the plurality of transistors.

24. (New) The transmission gate of Claim 21, wherein the switch circuit is a transistor, the input of the switch circuit is a source of the transistor, the output of the switch circuit is a drain of the transistor, and the control input of the switch circuit is a gate of the transistor, and wherein the

voltage difference between the control input voltage and the input voltage is the gate-to-source voltage of the transistor.

25. (New) The transmission gate of Claim 21, wherein:

the boost circuit is a charge pump circuit that is arranged to provide the boost voltage such that the boost voltage is greater than the supply voltage; and

wherein the current source circuit is a current mirror circuit that is arranged to provide the bias current such that the bias current is substantially constant.

26. (New) The transmission gate of Claim 21, wherein the constant voltage difference circuit is arranged to provide the control input voltage such that the control input voltage tracks the input voltage such that the voltage difference between the control input voltage and the input voltage is substantially constant, but such that the voltage difference varies slightly over temperature and process.

27. (New) The transmission gate of Claim 26, wherein the constant voltage difference circuit is arranged to provide the control input voltage such that the voltage difference between the control input voltage and the input voltage varies over temperature and process such that an on-resistance of the switch circuit between the input node and the output node is substantially constant over temperature and process.

28. (New) The transmission gate of Claim 21, wherein the constant voltage difference circuit includes:

a first transistor that is coupled between the control input node and another node, wherein the first transistor is arranged in a diode configuration; and

a second transistor including a gate that is coupled to the input node, a source that is coupled to the other node, and a drain.

29. (New) The transmission gate of Claim 28 wherein the current source circuit, the first transistor, and the second transistor are coupled in series.

30. (New) The transmission gate of Claim 28, wherein the first and second transistors are both p-type transistors.

31. (New) The transmission gate of Claim 28, wherein the switch circuit is a third transistor, the first transistor is an n-type transistor, the second transistor is a p-type transistor, the third transistor is an n-type transistor, and wherein the first transistor substantially matches the third transistor.

32. (New) The transmission gate of Claim 28, wherein the switch circuit is a third transistor, the input of the switch circuit is a source of the third transistor, the output of the switch circuit is a drain of the third transistor, the control input of the switch circuit is a gate of the third transistor, and wherein the first, second, and third transistors are sized sufficiently small that signals having a frequency of at least 1.5 GHz are capable of being transmitted from the input node to the output node during the on condition.

33. (New) A circuit for multiplexing, comprising:

a first transmission gate, including:

a switch circuit including an input that is coupled to an input node, an output that is coupled to an output node, and a control input that is coupled to a control input node; and

a constant voltage difference circuit that is coupled to the control input node, wherein the constant voltage difference circuit is arranged to provide a control input voltage at the control input node such that a voltage difference between the control input voltage and an input voltage at the input node is substantially constant during an on condition of the first transmission gate, and wherein the constant voltage difference circuit includes at least one of a first transistor and a first diode.

34. (New) The circuit of Claim 33, further comprising:

a second switch circuit including an input that is coupled to the input node, an output that is coupled to a second output node, and a control input that is coupled to a control input node.

35. (New) The circuit of Claim 33, further comprising:

a second transmission gate, including:

a second switch circuit including an input that is coupled to a second input node, an output that is coupled to the output node, and a control input that is coupled to a second control input node; and

a second constant voltage difference circuit that is coupled to the second control input node, wherein the second constant voltage difference circuit is arranged to provide a second control input voltage at the second control input node such that a voltage difference between the second control input voltage and a second input voltage at the second input node is substantially constant during an on condition of the second transmission gate.

36. (New) The circuit of Claim 35, wherein the second input voltage is a calibration voltage, the on condition of the second transmission gate occurs during a calibration phase, and an on condition of the first transmission gate occurs during a normal operation.

37. (New) The circuit of Claim 36, wherein:

the first transmission gate further includes:

a boost circuit that is arranged to provide a boost voltage at a boost node responsive to a supply voltage, such that the boost voltage is greater than the supply voltage;

a current source circuit that is coupled between the boost node and the control input node, wherein the current source circuit is arranged to provide a bias current that is substantially constant during the on condition of the first transmission gate;

the constant voltage difference circuit includes:

a first transistor that is coupled between the control input node and another node, wherein the first transistor is arranged in a diode configuration; and

a second transistor including a gate that is coupled to the input node, a source that is coupled to the other node, and a drain;

the switch circuit is a third transistor;

the input of the switch circuit is a source of the third transistor;

the output of the switch circuit is a drain of the third transistor; and

wherein the control input of the switch circuit is a gate of the third transistor.

38. (New) A method for multiplexing, comprising:

receiving an input voltage at an input node;

during an off condition, substantially de-coupling an output node from the input node;

providing a boost voltage; and

during an on condition:

providing a bias current responsive to the boost voltage; and

coupling the input signal to the output node by:

responsive to the bias current, providing a control input signal such that a voltage difference between the control input voltage and the input voltage is substantially constant; and

providing the control input signal to a control input of a switch circuit that is coupled between the input node and the output node.

39. (New) The method of Claim 38, wherein providing the control input voltage is further accomplished such that the voltage difference between the control input voltage and the input voltage varies over temperature and process such that an on-resistance of the switch circuit between the input node and the output node is substantially constant over temperature and process.

40. (New) The method of Claim 38, wherein providing the control input signal includes:

receiving the bias current at a control input node, wherein the control input of the switch circuit is coupled to the control input node;

employing a first gate-to-source voltage to provide a voltage drop between the control input node and another node;

employing a second gate-to-source voltage to provide a voltage drop between the other node and the input node.